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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,290	03/31/2006	Mitsuaki Osame	0756-7670	7471

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
11/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,290	OSAME ET AL.	
	Examiner	Art Unit	
	LONG NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-18 and 22-27* is/are pending in the application.

4a) Of the above claim(s) *7-18* is/are withdrawn from consideration.

5)☒ Claim(s) *22-24* is/are allowed.

6)☒ Claim(s) *1-4 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/7/09 has been entered.

Claim Objections

2. Claim 26 is objected to because of the following informalities: on line 1, "claim 1" should be changed to --claim 2-- to provide antecedent basis for "the multiple resistors". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagida Hiroyoshi (JP 08-107345-A).

With respect to claims 1 and 25, Figure 5 of Yanagida Hiroyoshi discloses a semiconductor device, which includes: a first transistor (Tr6), a plurality of inverters (1a); a first power source applying a first potential (Vcc); a second power source applying a second potential (Vss); a circuit (whichever circuitry that is used to generated VM connected to gate of transistor

Tr6) generating a third potential (VM) which is different from the first and second potentials (see Figure 3); wherein each of the plurality of inverters (1a) comprising: a second transistor and a third transistor (Tr1 and Tr2, see Figure 2); wherein each of the plurality of inverters (1a) is connected to the first power source (Vcc); wherein one of a source and a drain of the first transistor (Tr6) is connected to the second power source (Vss), wherein the other of the source and the drain of the first transistor (Tr6) is connected to each of the plurality of inverters (1a); wherein gate of the first transistor (Tr6) is connected to the circuit (circuitry generated VM), wherein a first signal (IN) is inputted to gates of the second and third transistors (input IN of inverters 1a) of each of the plurality of inverters (1a); wherein a second signal is output (OUT) from one of a source and a drain of the second transistor and one of a source and a drain of the third transistor of each of the plurality of inverters (output OUT of each inverter 1a, see also Figure 2); wherein the first potential (Vcc) is higher is than the second potential (Vss).

With respect to claim 3, Figure 5 of Yanagida Hiroyoshi discloses a semiconductor device, which includes: a first transistor (Tr7), a plurality of inverters (1a); a first power source applying a first potential (Vcc); a second power source applying a second potential (Vss); a circuit (whichever circuitry that is used to generated VM connected to gate of transistor Tr7) generating a third potential (VM) which is different from the first and second potentials (see Figure 3); wherein each of the plurality of inverters (1a) comprising: a second transistor and a third transistor (Tr1 and Tr2, see Figure 2); wherein one of a source and a drain of the first transistor (Tr7) is connected to the first power source (Vcc), wherein the other of the source and the drain of the first transistor (Tr6) is connected to each of the plurality of inverters (1a); wherein each of the plurality of inverters (1a) is connected to the second power source (Vss, by

way of Tr6, Figure 6); wherein gate of the first transistor (Tr7) is connected to the circuit (circuitry generated VM), wherein a first signal (IN) is inputted to gates of the second and third transistors (input IN of inverters 1a) of each of the plurality of inverters (1a); wherein a second signal is output (OUT) from one of a source and a drain of the second transistor and one of a source and a drain of the third transistor of each of the plurality of inverters (output OUT of each inverter 1a, see also Figure 2); wherein the first potential (Vcc) is higher is than the second potential (Vss).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 4, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagida Hiroyoshi (JP 08-107345-A) in view of Uchiki et al. (USP 6,646,486).

With respect to claim 2, 4, 26 and 28, Figure 5 of Yanagida Hiroyoshi teaches all the limitations of these claims as discussed in the 102 rejection above except for the circuit includes multiples resistors connected in series between the first power source and the second power source, wherein the third potential is outputted from a connecting node of two resistors that are selected from the multiple resistors, wherein each of the multiple resistors has a resistance which is constant regardless of a voltage applied thereto. However, Figure 12C of the Uchiki et al. teaches a voltage divider generator circuit that includes a plurality of resistors (R1, R2) connected in series between the first power source (Vdd) and the second power source (GND),

wherein the third potential (N1) is outputted from a connecting node (N1) of two resistors (R1, R2) that are selected from the multiple resistors, wherein each of the multiple resistors has a resistance which is constant regardless of a voltage applied thereto. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuitry of Yanagida Hiroyoshi by specifically using the voltage divider generator of Figure 12C to generate the third potential VM for Figure 5 of the Yanagida Hiroyoshi's circuitry for the purpose of easily achieving a known reference voltage based on the ratio of the fixed resistances of the resistors. Thus, this modification/combination meets all the limitations of claims 2, 4, 26 and 27.

Allowable Subject Matter

7. Claims 22-24 are presently allowed.

Response to Arguments

8. Applicant's arguments filed on 4/6/09 have been fully considered but they are not persuasive.

Applicant's arguments filed on 10/7/09 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816